Claims:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity;

an epitaxially formed semiconductor layer of a second conductivity formed over said substrate;

a body region of said first conductivity formed in said epitaxially formed semiconductor layer;

a source region of said second conductivity formed in said body region, said source region being adjacent an invertible channel in said body region;

a gate structure formed over said invertible channel region, said gate structure including a gate electrode which is spaced from said invertible channel by a gate insulation layer;

a drain region formed in said epitaxially formed semiconductor layer, said drain region and said body region being spaced from one another by a drift region in said epitaxially formed semiconductor layer; and

a field plate structure disposed over said drift region, said field plate structure including a first field plate disposed over a first insulation layer of a first thickness, a second field plate disposed over a second insulation layer of a second thickness, said second insulation layer being formed over said first insulation layer, and a third field plate spaced from said second field plate by a third insulation layer of a third thickness.

2. A semiconductor device according to claim 1, wherein said first insulation layer is comprised of an oxide.

3. A semiconductor device according to claim 1, wherein said first thickness is 0.4 microns.

4. A semiconductor device according to claim 1, wherein said second insulation layer is comprised of an oxide.

5. A semiconductor device according to claim 1, wherein said second thickness is 1.3 microns.

6. A semiconductor device according to claim 1, wherein said third insulation layer is comprised of an oxide.

7. A semiconductor device according to claim 1, wherein said third thickness is 1.4 microns.

8. A semiconductor device according to claim 1, wherein said first field plate extends from said gate electrode.

9. A semiconductor device according to claim 1, wherein said first field plate is comprised of conductive poly silicon.

10. A semiconductor device according to claim 1, wherein said second field plate is comprised of a first portion and a second portion, said first portion and said second portion being spaced from one another by a gap.

11. A semiconductor device according to claim 10, wherein said gap between said first portion of said second field plate and said second portion of said second field plate is 45 microns.

12. A semiconductor device according to claim 1, wherein said third field plate is comprised of a first portion and a second portion, said first and second portions being spaced from one another by a gap.

13. A semiconductor device according to claim 12, wherein said gap between said first portion of said third field plate and said second portion of said second field plate is 25 microns.

14. A semiconductor device according to claim 1, wherein said second field plate includes a first annular portion and a second annular portion, said annular portions being disposed around said drain region and spaced from one another by a gap.

15. A semiconductor device according to claim 14, wherein said gap between said first annular portion and said second annular portion of said second field plate is 45 microns.

16. A semiconductor device according to claim 1, wherein said third field plate includes a first annular portion and a second annular portion, said annular portions being disposed around said drain region and spaced from one another by a gap.

17. A semiconductor device according to claim 16, wherein said gap between said first annular portion and said second annular portion of said third field plate is 25 microns.

18. A semiconductor device according to claim 1, wherein said second field plate includes a first annular portion and a second annular portion, said annular portions being disposed around said drain region and spaced from one another by a first gap; said third field plate includes a first annular portion and a second annular portion, said annular portions being disposed around said drain region and spaced from one another by a second gap, said first gap being wider than said second gap.

19. A semiconductor device according to claim 18, wherein said first gap is about 45 microns and said second gap is about 25 microns.

20. A semiconductor device according to claim 18, wherein said first field plate terminates below said first portion of said second field plate.

21. A semiconductor device according to claim 18, wherein said second portion of said second field plate is electrically connected to said drain region, and to said second portion of said third field plate.

22. A semiconductor device according to claim 18, wherein said first portion of said second field plate is electrically connected to said first field plate.

23. A semiconductor device according to claim 18, wherein said first portion of said third field plate is electrically connected to said source region.

24. A semiconductor device according to claim 1, further comprising a resurf region of said first conductivity formed in said drift region below said field plate structure.

25. A field plate structure comprising:

a first field plate;

a second field plate disposed above and spaced from said first field plate; and

a third field plate disposed above and spaced from said second field plate.

26. A field plate structure according to claim 25, wherein said second field plate includes a first portion spaced from a second portion by a first gap, and said third field plate includes a first portion and a second portion spaced from said first portion by a second gap, said first gap being wider than said second gap.

27. A field plate structure according to claim 26, wherein said first portion and said second portion of each of said first and second field plates is annular.

28. A field plate structure according to claim 26, wherein said first portion of said second field plate is electrically connected to said first field plate and said second portion of said second field plate is electrically connected to said second portion of said third field plate.

29. A field plate structure according to claim 25, wherein said first field plate is insulated from said second field plate by an insulation layer and said second field plate is spaced from said third field plate by another insulation layer.